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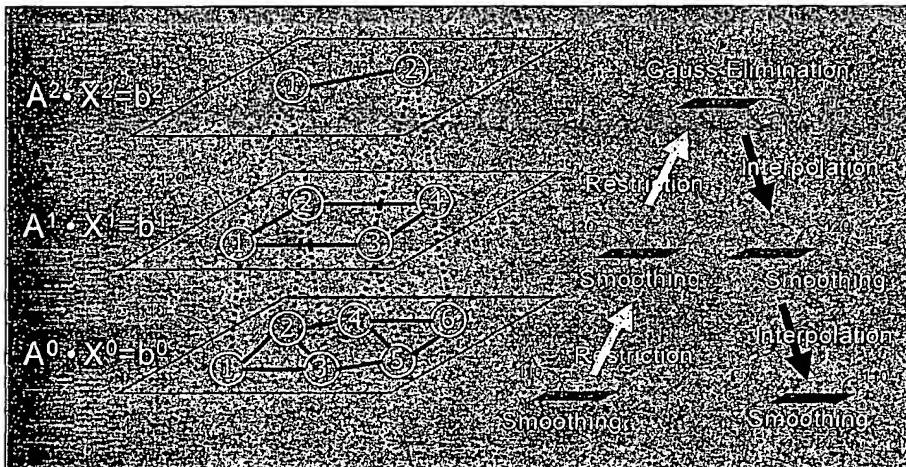
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- (71) Applicant (*for all designated States except US*): THE REGENTS OF THE UNIVERSITY OF CALIFORNIA [US/US]; 1111 Franklin Street, Oakland, CA 94607-5200 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (*for US only*): CHENG, Chung-Kuan [US/US]; 4407 Mensha Place, San Diego, CA 92130 (US). ZHU, Zhengyong [US/US]; 9152 F Regents Road, La Jolla, CA 92037 (US).
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(54) Title: CIRCUIT NETWORK ANALYSIS USING ALGEBRAIC MULTIGRID APPROACH



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(57) Abstract: This application describes techniques for applying an algebraic multigrid method to analysis of circuit networks with irregular and regular circuit patterns. Adaptive processing may be applied to the grid coarsening and error smoothing operations to increase the processing speed.

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**CIRCUIT NETWORK ANALYSIS USING ALGEBRAIC MULTIGRID APPROACH**

[0001] This application claims the benefit of U.S. Provisional Patent Application No. 60/475,069 entitled "CIRCUIT NETWORK ANALYSIS USING ADAPTIVE ALGEBRAIC MULTIGRID APPROACH" and filed on May 30, 2003, the entire disclosure of which is incorporated herein by reference as part of this application.

**Background**

10 [0002] This application relates to analysis of circuit networks such as power networks and clock networks and circuit simulation techniques.

[0003] Circuits may be viewed as networks of nodes and circuit components connected between nodes. As such, circuits may be analyzed based on a nodal analysis where a nodal equation may be written for each node based on the conversation of charge at the node, i.e., the total current entering the node is equal to the total current leaving the node (the Kirchoff's second rule). For a circuit with N nodes, N equations for the 15 N nodes can be expressed in terms of the properties of circuit components such as resistance, capacitance, and inductance, and in terms of the node voltages and currents. These N equations can be written into a matrix equation and are solved using various matrix approaches. For circuits with certain 20 control sources, inductance and current control sources, additional equations for different current branches may be 25 added to fully describe the circuits.

- [0004] Power network analysis may be performed based on the circuit matrix equations to investigate behaviors of circuit networks such as voltage drop, voltage oscillation, and electromigration. Excessive voltage drops may reduce the 5 switching speed as well as the noise margins of circuits and may even cause logic failures under some circumstances. Electromigration may decrease the chip lifetime. Moreover voltage oscillation may occur when power network resonance frequency drops to the range of the signal frequency.
- 10 [0005] One bottleneck of the power network analysis based on the above nodal analysis is the tremendous amount of variables in large power network such as an integrated circuit. One well-known circuit network analysis software program for solving such nodal equations is the SPICE circuit simulator 15 originally developed by the University of California at Berkeley. The SPICE uses the LU decomposition to solve the nodal equations for the node voltages. As the number of the circuit elements and nodes increases, the convergence of the LU deposition method and other direct methods slows down and 20 becomes inadequate for various circuits with a large number of circuit elements and nodes.
- [0006] Therefore, there is a need for power network analysis and circuit simulation techniques capable of analyzing circuits with large numbers of nodes and elements and produce 25 fast convergence.

Summary

[0007] The techniques described in this application apply an algebraic multigrid method to analysis of circuit networks.

In one implementation, for example, a method for analyzing a circuit network include representing a circuit network by

5 using a plurality of levels of grids with different numbers of nodes to represent the circuit network according to an algebraic multigrid method, applying a restriction mapping from one level to a next coarser level to propagate computation results of the one level to the next coarse level,

10 and applying an interpolation mapping from one level to a next finer level to propagate computation results of the one level to the next finer level. In each level, an iterative smoothing operation is performed to obtain computation results of each level comprising states of nodes in each level. The

15 above restriction mapping and the iterative smoothing operation from the finest level to the coarsest level and the interpolation mapping and the iterative smoothing operation from coarsest level back to the finest level are repeated for at least one time to obtain a solution to the circuit network.

20 [0008] As another example, a method for analyzing a circuit network includes the following steps. An algebraic multigrid method is applied to a matrix representative of a circuit network to construct a plurality of matrices with different degrees of coarsening grids. The regions in the circuit

25 network with active circuit activities are represented by

active grids and regions in the circuit network with less active circuit activities are represented by inactive grids.

- [0009] In yet another example, a method for analyzing a circuit network includes representing a circuit network by 5 using a matrix of nodes having fine nodes and coarse nodes and applying an adaptive coarse grid construction procedure to assign grid nodes in the matrix as either coarse grid nodes or fine grid nodes. This assignment is made according to (1) circuit activities and (2) a matrix structure of the matrix. 10 Next, iterative smoothing operations are applied at selected local fine grids corresponding to active regions at a finest level obtained in the adaptive coarse grid construction procedure.

[0010] Different from some other on-chip power grid analysis 15 methods that focus on IR-drop caused by the resistance of the power network, the exemplary analysis methods described here may include the contribution of the inductance of the circuit networks because such an effect becomes comparable with the contribution of the resistance when the signal frequency 20 increasing to a certain level. In addition, adaptive features in the grid coarsening and the error smoothing operations described here can significantly improve the processing speed.

[0011] These and other implementations, examples, and associated advantages are described in detail in the drawings, 25 the detailed description, and the claims.

Brief Description of Drawings

[0012] FIG. 1 illustrates an example of a three-level multigrid structure for a circuit network and the corresponding processing operations for mapping between 5 different levels and error smoothing at each level according to one implementation.

[0013] FIG. 2 illustrates an example of a linear RLC circuit network with an irregular spatial circuit pattern which is suitable for an algebraic multigrid analysis described in this 10 application.

[0014] FIGS. 3A and 3B illustrate examples of coarsening structures based on coarsening techniques described in this application.

[0015] FIG. 4 shows an example of an adaptive 3-level 15 multigrid structure for a circuit network in which a non-global active regions are applied to the finest grid level.

[0016] FIGS. 5A and 5B compare the transient analysis voltage waveforms of one node from SPICE and the present adaptive AMG approach.

20 Detailed Description

[0017] The network analysis methods described here are based on algebraic multigrid (AMG) methods described by W. L. Briggs in "A Multigrid Tutorial", SIAM 2000 and the Web site at <http://www.llnl.gov/casc/people/henson/mgtut/ps/mgtut.pdf>.

25 The AMG is a multigrid method and is an efficient technique for solving partial differential equations. The basic idea of

a multigrid method is to map the hard-to-damp low frequency error at fine level to easy-to-damp high frequency error at coarse level, solve the mapped problem at coarse level, and then map the error correction of coarse level back to fine 5 level. A hierarchical grid structure with multiple levels is constructed to perform such multigrid computations. At each level, a forward iterative smoothing operator such as Gauss-Seidel erases high frequency errors. There are two kinds of multigrid methods: the geometric multigrid and the algebraic 10 multigrid (AMG). The geometric multigrid method generally requires regular mesh structures. AMG does not require a regular mesh structure and can apply to other non-regular structures. In at least this regard, the AMG is a good alternative to the geometric multigrid method. The coarsening 15 and interpolation operations of the AMG are based on the matrix itself. This overhead may make the AMG less efficient than the geometric multigrid method if the problem analyzed has a regular mesh structure.

[0018] Many circuits, such as digital or mixed-signal 20 circuits, usually have irregular structures. The network analysis methods described here adopt the algebraic multigrid method and do not require a regular circuit pattern. Hence, circuits with irregular circuit patterns can be analyzed.

[0019] In another aspect, various other power grid analysis 25 techniques focus on voltage drops caused by resistance of the power network without analyzing the effects of the inductance

present in the network. As the signal frequency increases, the effects of the inductance of the on-chip power network become comparable with those of the resistance. Therefore, the effects of the inductance may no longer be ignored in 5 order to properly characterize the circuits. The network analysis methods described here based on the AMG may be designed to include the effects of the inductance such as the self and mutual inductances in the circuits. Accuracy of the present network analysis methods is checked and assured by 10 comparing the norm of residue with the user-defined error tolerance.

[0020] In addition, the network analysis methods described here perform the error smoothing operations in each of the multiple iterations through the multigrid cycles. The 15 iteration terminates only after the norm of the residue error is smaller than a pre-determined error tolerance level or threshold value.

[0021] Furthermore, the network analysis methods described here integrate adaptive grid structures and adaptive smoothing 20 operations to capture the multi-rate behavior and circuit latency in various networks. This adaptive design allows active circuit regions to be assigned with more computation in order to accurately capture the behavior of these regions and allows for inactive circuit regions to be assigned with less 25 computation to reduce the computation load. The circuit spatial and temporal latency are fully explored along with the

multi-rate behavior to avoid any unnecessary computation without losing accuracy and convergence of the analysis. The present methods also have the ability to analyze coupling effects with electromagnetic retardations for high-frequency 5 chip-package-board scale analysis. Hence, as one example, the effects of inductance in the circuits can be included in the analysis.

[0022] A general circuit network with N nodes may be mathematically represented a matrix equation after the 10 integral approximation:

$$A^0 x = b,$$

where x is a vector of node voltages, b is a matrix that 15 represents effects of current sources in the circuit network and contributions from solutions of previous time points, and the matrix  $A^0$  represents the spatial structure of the circuit network. For a circuit with a large number of nodes, the matrix  $A^0$  is large and it may be computationally complex to 20 solve the matrix equation for the node voltages in x.

[0023] Based on the AMG concept, the circuit network represented by the matrix A may be "coarsened" into one or more simplified hierarchical grids representing circuit networks of different levels of coarsening with reduced number 25 of nodes, such as  $A^1$ ,  $A^2$ , etc. The first level coarsened circuit network,  $A_1$ , for example, may use one node to

represent two or more nodes within a circuit region in the original circuit network A0. The second level coarsened circuit network, A2, may use one node to represent two or more nodes in a circuit region in the first level coarsened circuit 5 network A1. Instead of directly solving the large matrix equation  $A^0x=b$ , multiple levels of circuit networks A0, A1, and A2 are solved in an iterative manner to propagate residual errors to be removed by iterative smoothing from one grid to the next coarser grid and to use the solutions of one as the 10 initial solutions for the next finer grid. For example, certain low spatial frequency errors may be smoothed at the coarse levels A0 and A1 while some high spatial frequency errors may be smoothed at the coarsest level A2. In this example, the original matrix equation is essentially converted 15 into three matrix equations with different levels of coarsening in their circuit spatial structures:

$$A_0x_0=b_0$$

$$A_1x_1=b_1$$

$$20 \quad A_2x_2=b_2.$$

The residual errors are propagated from A0 to A1 and finally to A2 through restriction mapping while the solutions are propagated from A2 to A1 and finally to A0 through 25 interpolation mapping. For one single iteration cycle, the computation may follow the following mapping routine:

A0→A1→A2→A1→A0.

Certainly, more than 3 levels of coarsening may be  
5 implemented. It is noted that the computation for solving  
A0x0=b0 here is different from directly solving the original  
matrix equation A0x=b due to the mapping.

[0024] FIG. 1 illustrates one example of the above multigrid  
mapping. The plane 110 represents the original circuit  
10 network A0 before any coarsening where 5 nodes are shown. The  
plane 120 represents a first coarsened circuit network (A1)  
where node 1 in A1 is mapped from node 1 on A0, node 2 on A1  
is mapped from nodes 2 and 3 on A0, etc. The plane 130  
represents a second coarsened circuit network (A2) based on  
15 A1, where the node 1 on A2 is mapped from nodes 1 and 2 on A1  
and node 2 on A2 is mapped from nodes 3 and 4 on A1. The  
mapping from one level grid (e.g., A1) to a coarser level grid  
(e.g., A2) is a restriction. The mapping from one level grid  
(e.g., A1) to a finer level grid (e.g., A0) is an  
20 interpolation. At each level, an iterative solver is used to  
solve the matrix equation at that level and to smooth the  
errors. The residual error from each level is the absolute  
value of the difference between A0x0 and b0 for A0, A1x1 and  
b1 for A1, or A2x2 and b2 for A2. The residual error is  
25 mapped along with the nodes to the next coarser level so that  
the errors are continuously smoothed.

- [0025] FIG. 1 further shows the computation process in the flowchart on the right hand side. Smoothing is performed at each level in the restriction process from the finest level to the coarsest level and in the interpolation process from the 5 coarsest level to the finest level. Hence, errors with high spatial frequencies that are not reduced at the fine levels will be smoothed at the coarse level. In particular, the cycle is repeated until the residual error falls below a pre-determined threshold value.
- 10 [0026] The computations in a single multigrid cycle shown in FIG. 1 may be mathematically described as follows in a single V-cycle scheme. The mapping operator from a fine level to a coarse level is called restriction operator  $I_h^u$ . A coarse to fine level mapping operator is called interpolation operator  $I_h^u$ . The system matrix equation  $A^h u^h = f^h$  is solved hierarchically 15 at different levels; the superscript refers to the level of the grid structure.

Single V-Cycle Scheme:  $V^h \leftarrow V^h(v^h, f^h)$

- 20 • Relax on  $A^h u^h = f^h$  for  $v_1$  times with an initial guess  $v^h$  as the solution
- compute the residue:  $r^h = f^h - A^h u^h$
- Compute  $f^{2h} = I_h^{2h} r^h$  (restriction mapping)
- Relax on  $A^{2h} u^{2h} = f^{2h}$  for  $v_1$  times with an initial 25 guess  $v^{2h} = 0$ ,  $r^{2h} = f^{2h} - A^{2h} u^{2h}$

- o Compute  $f^{4h} = I_{2h}^{4h} r^{2h}$  (restriction mapping)
    - Relax on  $A^{4h}u^{4h} = f^{4h}$  for  $v_1$  times with an initial guess  $v^{4h} = 0$ ,
    - Compute residue  $r^{4h} = f^{4h} - A^{4h}u^{4h}$
    - Compute  $f^{8h} = I_{4h}^{8h} r^{4h}$ 
      - 
      - 
      - to coarsest level .
      - 
      -
    - Correct  $u^{4h} \leftarrow u^{4h} + I_{8h}^{4h} u^{8h}$  (Interpolation mapping)
    - Relax on  $A^{4h}u^{4h} = f^{4h}$  for  $v_2$  times with an initial guess  $u^{4h}$ 
      - o Correct  $u^{2h} \leftarrow u^{2h} + I_{4h}^{2h} u^{4h}$  (interpolation mapping)
      - o Relax on  $A^{2h}u^{2h} = f^{2h}$  for  $v_2$  times with initial guess  $u^{2h}$ 
        - Correct  $u^h \leftarrow u^h + I_{2h}^h u^{2h}$  (interpolation mapping)
        - Relax on  $A^h u^h = f^h$  for  $v_2$  times with initial guess  $u^h$
- 10
- 15
  - 20 In the above example, the matrix,  $I^l$  ( $l=h, 2h, 4h, 8h$ , etc.), represents the mapping operation from one level to an adjacent level, and  $r^l$  represents the residual error at the level  $l$  ( $=h, 2h, 4h, 8h$ , etc.). The mapping operator  $I^l$  from

fine to coarse level is called restriction operator, and a mapping operator from coarse to fine level is called an interpolation operator. The parameters  $v_1$  and  $v_2$  are constant numbers for the number of iterations at different 5 levels.

[0027] The basic idea of the above multigrid approach is to map the hard-to-damp low frequency errors at a fine level to easy-to-damp high frequency errors at a coarse level, solve the mapped problem at coarse level, and then map the error 10 correction of the coarse level back to the fine level. At the fine level, the high-frequency errors that are not erased by the smoothing at the coarse level are smoothed out.

Therefore, errors with different spatial frequencies are smoothed out through the operations at different levels. At 15 each level, the high frequency error for that level is erased by a smoothing operator that is a forward iterative method such as the Gauss-Seidel method.

[0028] The number of the levels of grids is selected based on the specific layouts and properties of circuit networks. In 20 one implementation, for example, the construction of hierarchical grid structure stops at the level when the reduced matrix can be quickly solved by a direct solving method such as a Gaussian elimination method. For example, the LU decomposition or factorization method, which is an 25 extension of the Gaussian elimination, may be used to find the coarsest level. Once the exact solution of the problem at the

- coarsest level is found, the interpolation is performed from the coarsest level back to the finest grid, i.e., the original circuit grid, by interpolation from one level to a next finer level and smoothing operation at each level. An iteration of 5 restriction from the fine grid to the coarsest grid and interpolation from the coarsest grid back to the fine grid is called a single multigrid cycle, which will iterate several times till the solution converges when the residual error is reduced below a threshold.
- 10 [0029] The network analysis methods described here may use different models for different circuit components. For circuits with passive circuit elements exhibiting resistance (R) and capacitance (C) without conductance (L), the system equation for the circuits may be formulated as

15

$$C\dot{X}(t) + GX(t) = U(t) \quad (2.1)$$

- where X is the vector of the nodal voltages and G is the conductance ( $1/R$ ), U(t) represents the current from a 20 current source. Applying trapezoidal approximation with a time step of h to equation (2.1) produces the following:

$$(G + \frac{2}{h}C)X(t+h) = -(G - \frac{2}{h}C)X(t) + U(t) + U(t+h)$$

(2.2)

25

The left hand side matrix in (2.2) is symmetric and positive definite which makes the iterative methods converge quickly.

[0030] When inductance is included, the system matrix equation may be written as follows:

$$5 \quad \hat{C}\dot{\hat{X}}(t) + \hat{G}\hat{X}(t) = \hat{U}(t) \quad (2.3)$$

where  $\hat{C} = \begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix}$ ,  $\hat{X} = \begin{bmatrix} V \\ I \end{bmatrix}$ ,  $\hat{U} = \begin{bmatrix} U \\ 0 \end{bmatrix}$  and  $\hat{G} = \begin{bmatrix} G & -A_l^T \\ A_l & 0 \end{bmatrix}$

Equation (2.3) can be rewritten as:

10

$$\begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} \begin{bmatrix} V \\ I \end{bmatrix} + \begin{bmatrix} G & -A_l^T \\ A_l & 0 \end{bmatrix} \begin{bmatrix} V \\ I \end{bmatrix} = \begin{bmatrix} U \\ 0 \end{bmatrix} \quad (2.4)$$

Applying trapezoidal approximation with time step  $h$ , the solution of equation (2.4) is derived by

15

$$\begin{bmatrix} \frac{2C}{h} + G & -A_l^T \\ A_l & \frac{2L}{h} \end{bmatrix} \begin{bmatrix} V(t+h) \\ I(t+h) \end{bmatrix} = \begin{bmatrix} \frac{2C}{h} - G & A_l^T \\ -A_l & \frac{2L}{h} \end{bmatrix} \begin{bmatrix} V(t) \\ I(t) \end{bmatrix} + \begin{bmatrix} U(t+h) + U(t) \\ 0 \end{bmatrix} \quad (2.5)$$

Although the modified nodal analysis (MNA) method can handle elements without the description of the admittance, the transient analysis system matrix in (2.5) is no longer symmetric and positive definite when the inductance is included because of the introduction of current variables. Since Multigrid and the PCG method require the matrix to be symmetric positive definite, some extra processing is needed

to reformulate the system. Accordingly, the variable vector is split into a nodal voltage vector and a branch current vector. Using block matrix operations, the Equation (2.5) can be decomposed into two iteration formulas for nodal voltages and branch currents, respectively:

$$\Rightarrow \begin{cases} \left( \frac{2C}{h} + G - \frac{h}{2} A_l^T L^{-1} A_l \right) V(t+h) = \\ \left( \frac{2C}{h} - G + \frac{h}{2} A_l^T L^{-1} A_l \right) V(t) + [U(t) + U(t+h)] + 2A_l^T I(T) \\ I(t+h) = I(t) - \frac{h}{2} L^{-1} A_l [V(t+h) + V(t)] \end{cases} \quad (2.6)$$

In Equation (2.6),  $L^{-1}$  corresponds to the K matrix in A. Devgan, et al., "How to Efficiently Capture On-Chip Inductance Effects: Introducing a New Circuit Element K", IEEE/ACM International Conference on Computer Aided, pp 150-155 (November 2000). The matrix inversion overhead is reduced by sparsification methods. If the inductance matrix is symmetric and positive definite (S.P.D.), the system matrix is still S.P.D. This condition also holds for forward Euler, backward Euler integration approximation methods. Note that the topology of reformulated system matrix in (2.6) is no longer the same as original circuit topology. Geometric based coarse grid reduction algorithm cannot be applied to RLC network directly.

[0031] As an example for power source networks, a power source network may have separated power and ground. In many

applications, a power network may have an irregular mesh as shown in FIG. 2. Every intersection node may have a ground capacitance. Between neighboring intersection nodes is a resistor, or a resistor and a inductor in series. Mutual inductance can also be included. The devices with activities can be modeled as time-varying current sources.

[0032] The AMG method has no grid concept. In adopting the AMG approach, the network analysis methods described here determine the exact expressions of the inter-level mapping operators, i.e., the restriction and interpolation, based on the original matrix A for the particular circuit network of interest. In AMG, a smooth error means error components with relatively small residuals. See, e.g., the cited tutorial by Briggs. Hence, after several iterations of the smoothing operation, the residue is small but the error decreases slowly: .

$$Ae \approx 0$$

(3.1)

where e denotes the algebraic error vector and is a difference between the vector u and its approximation vector v. Equation (3.1) can be rewritten as follows:

$$a_u e_i \approx - \sum_{j \neq i} a_{ij} e_j$$

(3.2)

Hence the error of a fine node can be well represented by linear combinations of its neighbors' errors.

[0033] If coarse and fine nodes have already been defined, the error of the fine node may be approximated by errors of only 5 its coarse node neighbors for an interpolation process.

Certainly, other interpolation methods may be used. This simple approach works well for the power grid problem. From Equation (3.2), the interpolation operator  $I_{2h}^h$  can be constructed. The mapping between levels in two directions are 10 symmetric and therefore the restriction operator  $I_h^{2h}$  can be obtained by the transposition of the interpolation operator, i.e.  $I_{2h}^{hT} = I_h^{2h}$ . Accordingly, the coarse level matrix can be computed as  $A^{2h} = I_{2h}^h A^h I_h^{2h}$ . As a result, the coarse level matrix  $A^{2h}$  remains symmetric positive definite. If the matrix is 15 symmetric and positive definite, the convergence of AMG can be guaranteed as long as the smoothing operation converges at each level. A detailed proof for this can be found in, e.g., K. Stuben, "Algebraic Multigrid: An Introduction with Applications", GMD Report No.53 (March 1999).

[0034] In some power grid networks, the RLC values may be 20 uniform at the same layer. Due to the non-uniform power densities and the timing of the switching events, the power supply noise may exhibit a spatial variation. Therefore, some nodes of the power network may have more rapid nodal voltage 25 changes than other nodes. These nodes with rapid changes are more active than the rest nodes of the circuit network.

[0035] Because of such differences in node activities, the nodes in the circuit network are not computationally equal in the sense that the rapid changes in "active" nodes should be monitored and analyzed more accurately to adequately model 5 their behavior than the relatively slow changes in "inactive" nodes in order. This different computational treatments can be used to accurately characterize the circuit network, to achieve fast convergence in the computation, and to reduce unnecessary computation. In recognition of above, the network 10 analysis methods described here may be implemented in a way to be "adaptive" in applying the multigrid coarsening so that active regions have finer grid structures than inactive regions.

[0036] In implementing the adaptive coarsening scheme in the 15 multigrid framework, active regions are assigned with relatively finer grids at a coarse level. The coarse grid nodes can be determined adaptively by the circuit activities as well as by the matrix representation of the circuit network (i.e., the spatial structure of the circuit). The coarse grid 20 may include two kinds of nodes: non-adaptive and adaptive coarse nodes. Non-adaptive coarse nodes are selected by a coloring scheme according to the matrix. Adaptive coarse nodes can be determined by the circuit activities.

[0037] The selection of non-adaptive coarse nodes may use a 25 two-level coloring scheme at every level of the hierarchical multigrid structure except the coarsest level. Initially, at

a given level of the grid other than the coarsest grid, the potential of each node is set to its degree, i.e., the number of directly connected neighboring nodes. The node with the maximum potential (the maximal directly connected neighboring nodes) is selected to be a coarse node (the first coarse node) and all its unassigned neighboring nodes are set as fine nodes. Next, for each newly set fine node, the potential of every neighboring node of such a fine node is increased by 1. At this time, among the currently unassigned nodes, the node with the maximum potential is selected as the second coarse node and its directly connected neighboring nodes are set as fine nodes. This process is repeated until every node has been assigned as a fine or coarse node. At the end, each fine node has at least one neighboring coarse node. This assignment of fine and coarse nodes at each level is made regardless of the circuit activities. Fine and coarse nodes are graphically represented by two different colors and thus this method of assigning nodes is called two color scheme.

[0038] Adaptive coarse nodes can be selected according to the activities of circuits. One suitable candidate for the measurement of the impact of circuit activities is the first order derivative of nodal voltages. As an example, the first order derivatives of nodal voltages for a RLC network shown in FIG. 2 may be approximated from Equation (2.4). Since not every node has a ground capacitor, the voltage vector  $V$  may be split into two separate voltage vectors  $V_1$  and  $V_2$ , where  $V_1$  is

the set of nodes each with a ground capacitor and V<sub>2</sub> is the set of nodes between resistance and inductance in branches. The first order derivative of the nodal voltage in V<sub>1</sub> can be calculated as follows. From Equation (2.4), the following can 5 be derived:

$$\begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} \begin{bmatrix} \dot{V}_1 \\ \dot{V}_2 \end{bmatrix} = -\begin{bmatrix} G_{11} & G_{12} & -A_{11}^T \\ G_{21} & G_{22} & -A_{12}^T \\ A_{11} & A_{12} & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ I \end{bmatrix} + \begin{bmatrix} U \\ 0 \\ 0 \end{bmatrix} \quad (4.1)$$

The first order derivative of intersection node voltage can be 10 approximated as

$$\dot{V}_1(t+h) = -C^{-1}[G_{11}V_1(t) + G_{12}V_2(t) - A_{11}^T I(t) + U(t+h)] \quad (4.2)$$

The inversion of the capacitance matrix can be readily 15 achieved because the capacitance matrix is actually a diagonal matrix. In this particular implementation, the nodes with relatively large voltage derivatives are "active" and thus are selected as adaptive coarse nodes. A threshold value for the first-order derivative may be selected, so that nodes with 20 first-order derivatives greater than the threshold can be selected as adaptive coarse nodes.

[0039] In some implementations, this adaptive coarsening based on circuit activities may be applied at the finest level of the hierarchical multigrid structure. The coarse grid 25 selection at other levels may be determined solely by the

coloring scheme in part because active components with finer first level coarse grid will still have relatively finer grid on the next coarse levels.

[0040] FIGS. 3A and 3B show examples of non-adaptive and 5 adaptive coarsening structures, respectively, where FIG. 3A shows a non-adaptive coarsening structure and FIG. 3B shows an adaptive coarsening structure. The grey scale of the color increases with the degree of the coarsening so that a fine level is represented by a light color and a coarse level is 10 presented by a dark color.. The darker color indicates the coarser a level in the grid structure is. In FIG. 3A, three different colors represent three different grid levels. In FIG. 3B, the coarsening structure solely based on the two-level coloring scheme are modified at each coarsening level 15 based on the circuit activities. In this particular example, the circuit activities apparently concentrate in the up-right corner of the circuit and therefore more adaptive coarse nodes are selected in this region. An active region has finer grid than the other region in every grid level.

20 [0041] FIG. 3A shows the nodes in the finest grid which includes all coarse nodes (adaptive and non-adaptive) and fine nodes. A coarse grid based on the finest grid in FIG. 3A may include only the coarse nodes. For example, the medium grey nodes may represent nodes in the grid A1 shown in FIG. 1 and 25 the dark grey nodes may represent nodes in the grid A2, the

coarsest grid, in FIG. 1. FIG. 3B shows the finest grid A0 with adaptive coarse nodes. Coarse nodes

[0042] Many circuits display spatial and temporal latency as well as multi-rate behaviors. Spatial latency in this context 5 means only part of a circuit network has activities at any time point while other parts of the circuit network are inactive. Temporal latency in this context refers to the situation where a given portion of the circuit network is active in some periods but inactive in other periods. The 10 multi-rate behaviors refer to active portions of a circuit network have various change rates in their currents and voltages.

[0043] Hence, additional "adaptive" features may be implemented in the present network analysis methods to avoid 15 or reduce certain unnecessary computations based on the spatial and temporal latency as well as multi-rate behaviors. As an example, different regions of a circuit network may be simulated with various time step sizes according to their 20 activities. This may be carried out without imposing a minimum time step size to the entire circuits for the sake of convergence. Referring back to FIG. 1, simulations of these different regions are not separated from other regions of the circuit network due to the multigrid restrictions and 25 interpolations throughout different levels. This is different from various partition-based commercial fast simulators which use variations in the time step sizes for each subcircuit and

solve each subcircuit separately. Such commercial simulators may reduce the computation overhead but suffer poor convergence and the difficulties in capturing mutual inductance coupling effect correctly.

5 [0044] The network analysis methods described here may incorporate adaptive grid structures and adaptive smoothing operations to capture the multi-rate behavior and circuit latency. Active regions may be assigned with relatively finer grid structures and are subject to more error smoothing 10 operations than inactive regions. The convergence can be guaranteed by the use of the multigrid method because the multigrid converges as long as smoothing operations at each level can damp the high frequency error.

[0045] As an example, the global fine grid at the finest 15 level may be reduced to several local fine grids corresponding to active regions and iterate the smoothing operations only inside these local fine grids. This technique can be used to avoid or reduce the unnecessary computation for inactive regions. This non-global coarsening may also be applied to 20 other coarsening grid levels other than the finest level. Hence, the multi-grid structure may have two or more levels of non-global grids. As described above, the active regions may be detected by the first order derivative of nodal voltages. Relying on the adaptive grid structure and adaptive smoothing, 25 different "time step sizes" may be used for active and inactive subcircuits in the sense that inactive subcircuits

may be subject to error smoothing operations at the finest level once every several time points. As a result, iterative smoothing operations are performed in active regions more frequently in time than in inactive regions.

5 [0046] FIG. 4 illustrates an example of configuration changes over time for an adaptive three-level coarsening multigrid structure for a circuit network. The multigrid structures with three levels 110, 120, and 130 at four different times t<sub>1</sub>, t<sub>2</sub>, t<sub>3</sub>, and t<sub>4</sub> are shown. Active regions in the finest grid level 110 are shown as local fine grid regions. Such a non-global finest grid level is "adaptive" to changes in the circuit activities. At time t<sub>1</sub>, the finest grid level has 3 active regions. At t<sub>2</sub>, however, there is only one active region. At times t<sub>3</sub> and t<sub>4</sub>, the active regions of the circuit 10 network further change. As the active regions changes, the multigrid structure change accordingly as illustrated. In one implementation, the iterative smoothing operation is performed locally in the active regions only in the finest level 110 but is performed globally over all nodes in the coarse levels 120 and 130. The coarsening structures at levels 120 and 120 are 15 also changed dynamically with the circuit network.

[0047] Such "adaptive" features in multigrid simulations may be applied to both linear circuits. If a node voltage change in a linear network (power or clock network) between time 20 points is less than a threshold M, this node is considered as an idle node. For active portions, different levels of

thresholds may be defined to determine various degrees of activities that results in multi local fine levels of grid structures.

[0048] The above multigrid circuit simulations without adaptive features and with adaptive features were implemented in ANSI C and were executed on a SUN Blade100 (300MHz) workstation with a 2-GB memory. The number of pre-smoothing and post-smoothing iteration were set to 3 at each level and the multigrid iteration termination control residue norm was set at  $1 \times 10^{-10}$ . At each grid level, the Gauss-Seidel method was used as the smoothing operator.

TABLE 1

Nodes	SPICE	AMG	Speedup
1706	1.68	0.17	9.8
2637	3.91	0.28	14
5105	15.01	0.57	26.3
10322	54.44	0.98	55.5
40842	708.22	3.93	180.2
91562	X	8.98	

15

TABLE 2

Nodes	SPICE	AMG	Adaptive AMG	Adaptive Speedup
1706	18.06	1.36	1.36	13.2
2637	41.23	4.08	3.78	10.9
5105	122.1	9.13	8.89	13.7
10322	456.42	18.7	18.1	25.2
40842	5048.5	165.1	155.2	32.5

[0049] Table 1 lists results of the DC analysis runtime of SPICE3 and the present AMG method without adaptive features. The results suggest that the present AMG method is more than

100 times faster than SPICE3 for large circuits. Table 2 compares the transient analysis runtime of SPICE3, non-adaptive AMG, and adaptive AMG. The time-varying currents were modeled as triangular waveforms with 2mA peak current and 5 40ps rising and falling time. Details of such modeling may be found, e.g., in S. Zhao, K. Roy, C. K. Koh "Frequency domain analysis of switching noise on power supply network," IEEE/ACM International Conference on Computer Aided Design (2000). Current sources were not evenly distributed and the timings 10 were also different. The transient analysis was conducted for a time duration of 5 ns. Experimental results show that adaptive AMG is faster than non-Adaptive AMG. The speedup against the non-adaptive AMG is not very obvious in part because the adaptive grid structure was applied to achieve 15 fast convergence and the smoothing operations were not made to be adaptive. Additional improvement in speed is expected when the adaptive concept is further applied to smoothing operations at each level. Our approach runs about 20 times faster than SPICE3 for the transient analysis. The 20 performance speedup is comparable with the PCG approach published by T. Chen and C. Chen in "Efficient Large-Scale Power Grid Analysis Based on Preconditioned Krylov-Subspace Iterative Methods", IEEE/ACM Design Automation Conference (2001).

25 [0050] Our tests suggest that the number of multigrid iterations dose not increase rapidly with the problem size and

the number of iterations appears to be independent of the problem size.

[0051] FIGS. 5A and 5B compare the transient analysis voltage waveforms of one node from SPICE (FIG. 5A) and the present 5 adaptive AMG approach (FIG. 5B). The waveforms are almost the same.

[0052] In implementations, the above described multigrid techniques and their variations may be implemented as computer software instructions. Such instructions may be stored on one 10 or more machine-readable storage media or devices and are executed by, e.g., one or more computer processors, or cause the machine, to perform the circuit analysis.

[0053] Only a few implementations are disclosed. However, it is understood that variations and enhancements may be made.

Claims

What is claimed is:

1. A method for analyzing a circuit network, comprising:
  - 5 representing a circuit network by using a matrix of nodes having fine nodes and coarse nodes;
  - applying an adaptive coarse grid construction procedure to assign grid nodes in the matrix as either coarse grid nodes or fine grid nodes according to (1) circuit activities and (2)
  - 10 a matrix structure of the matrix to construct a plurality of levels of grids with different numbers of nodes to respectively represent the circuit network; and
  - applying iterative smoothing operations at selected local fine grids corresponding to active regions at a finest level
  - 15 obtained in the adaptive coarse grid construction procedure.
2. The method as in 1, wherein the coarse grid nodes are divided into non-adaptive coarse nodes which are selected according to the matrix structure, and adaptive coarse nodes
- 20 which are selected according to circuit activities.
3. The method as in claim 2, wherein, in assigning non-adaptive coarse nodes, a node with a maximum potential in its degree is selected as a first non-adaptive coarse node and
- 25 each neighboring node of the first non-adaptive coarse node is temporality assigned as a fine node, and wherein a potential

of each neighboring node of the first non-adaptive coarse node is increased by one unit before a next level of assigning coarse and fine grid nodes so that each fine node has at least one neighboring coarse node upon completion of assigning non-  
5 adaptive coarse nodes.

4. The method as in claim 2, wherein an adaptive coarse node is selected according to a first-order derivative of a nodal voltage.

10

5. The method as in claim 4, wherein a coarse node is selected as an adaptive coarse node when the first-order derivative the coarse node is greater than a threshold value.

15

6. The method as in claim 5, further comprising selecting adaptive coarse nodes in a level that is not the finest level.

7.

The method as in claim 1, after the iterative smoothing operations in a level, further comprising:

20

applying a restriction mapping of nodes in the level to a next level with less nodes;

performing iterative smoothing operations again at the next level; and

25

repeating the restriction mapping and the iterative smoothing operations until reaching a level of nodes which are

solvable by a direct matrix solving method such as a Gaussian elimination method.

8. The method as in claim 1, after the iterative smoothing operations in a level, further comprising:
  - applying an interpolation mapping of nodes in the level to a next level with more nodes;
  - performing iterative smoothing operations again at the next level; and
- 10 repeating the interpolation mapping and the iterative smoothing operations until reaching the finest level of nodes.

9. The method as in claim 8, further comprising:
  - computing a residual value of an error after the iterative smoothing operations at the finest level;
  - comparing the residual value to a pre-determined threshold;
  - terminating any further processing when the residual value is less than the threshold; and
- 20 when residual value is greater than the threshold, the method further comprising:
  - applying a restriction mapping of nodes in the finest level to a next coarser level with less nodes,
  - performing iterative smoothing operations again at the next coarser level; and

repeating the restriction mapping and the iterative smoothing operations until reaching a coarsest level of nodes which is solvable by a direct matrix solving method such as a Gaussian elimination method,

5 applying an interpolation mapping of nodes in the coarsest level to a next finer level with more nodes,

performing iterative smoothing operations at the next finer level,

repeating the interpolation mapping and the iterative 10 smoothing operations until reaching the finest level of nodes, and

repeating the restriction mapping, the interpolation mapping and the respective iterative smoothing operation at different levels until the residual value at the finest level 15 is less than the threshold.

10. The method as in claim 1, further comprising dynamically changing designations of active and inactive regions of the circuit network according to circuit activities 20 at different times.

11. The method as in claim 10, further comprising applying iterative smoothing operations in active regions more frequently in time than in inactive regions.

12. The method as in claim 1, further comprising: in a passive linear circuit, applying different models to passive circuits exhibiting resistance and capacitance without inductance and passive circuits exhibiting inductance.

5

13. The method as in claim 12, further comprising separating nodal voltages and branch currents into different vectors during processing to make a system matrix to be symmetric and positive definite.

10

14. A method for analyzing a circuit network, comprising:  
representing a circuit network by using a plurality of levels of grids with different numbers of nodes to represent the circuit network according to an algebraic multigrid  
15 method;

applying a restriction mapping from one level to a next coarser level to propagate computation results of the one level to the next coarse level;

20 applying an interpolation mapping from one level to a next finer level to propagate computation results of the one level to the next finer level;

performing an iterative smoothing operation at each level to obtain computation results of each level comprising states of nodes in each level; and

25 repeating (1) the restriction mapping and the iterative smoothing operation from the finest level to the coarsest

level and (2) the interpolation mapping and the iterative smoothing operation from coarsest level back to the finest level for at least one time to obtain a solution to the circuit network.

5

15. The method as in claim 14, wherein the coarsest level is a level where a matrix equation for nodes in the level is solvable by a direct matrix method such as the Gaussian elimination method.

10

16. The method as in claim 14, wherein at least one level includes nodes corresponding to only selected circuit regions in the circuit network that are active and does not include nodes corresponding to inactive circuit regions in the circuit  
15 network.

15

17. The method as in claim 14, further comprising:  
assigning regions in the finest level with nodes corresponding to active circuit regions in the circuit network  
20 as active local fine grids; and  
performing the iterative smoothing operation only in the active local fine grids in the finest level to obtain computation results of the finest level.

25

18. The method as in claim 14, further comprising:

assigning regions in a level with nodes corresponding to active circuit regions in the circuit network as active local grids and other regions in that level as in inactive grids; and

- 5 performing the interactive smoothing operation in an active local grid more frequently than in an inactive grid.

19. The method as in claim 14, further comprising  
10 applying an adaptive coarse grid construction procedure to assign grid nodes in the matrix as either coarse grid nodes or fine grid nodes.

20. The method as in claim 19, wherein a coarse node is  
15 assigned by:

assigning a node with a maximum potential to its degree as a first coarse node and all neighboring nodes as initial fine nodes;

- for each of the initial fine nodes, increasing a  
20 potential of each of neighboring nodes by one unit;

assigning a node which has a maximum potential among other nodes except for the first coarse node as a second coarse node; and

- repeating the assigning for nodes that are not assigned  
25 as coarse nodes until all nodes are assigned.

21. The method as in claim 19, wherein the coarse nodes are selected according to their values of a first-order derivative of a nodal voltage.

5        22. A method for analyzing a circuit network, comprising:  
            applying an algebraic multigrid method to a matrix representative of a circuit network to construct a plurality of matrices with different degrees of coarsening grids;  
            representing regions in the circuit network exhibiting  
10     active circuit activities with active grids and regions in the circuit network exhibiting less active circuit activities with inactive grids; and  
            performing an iterative smoothing operation in an active grid more frequently than in an inactive grid to reduce an  
15     amount of computation.

23. The method as in claim 22, further comprising:  
            applying a restriction mapping of nodes in a coarse grid to a next coarser grid;  
20     performing the iterative smoothing operation at the next coarser grid; and  
            repeating the restriction mapping and the iterative smoothing operation until reaching the coarsest grid which has a matrix equation that is solvable by a direct matrix solving  
25     method such as a Gaussian elimination method.

23. The method as in claim 22, further comprising:

applying an interpolation mapping of nodes in one grid to  
a next finer grid;

5 performing the iterative smoothing operation at the next  
finer level; and

repeating the interpolation mapping and the iterative  
smoothing operation until reaching the finest grid.

25. An article comprising a machine-readable medium that  
10 stores machine-executable instructions, the instructions  
causing a machine to:

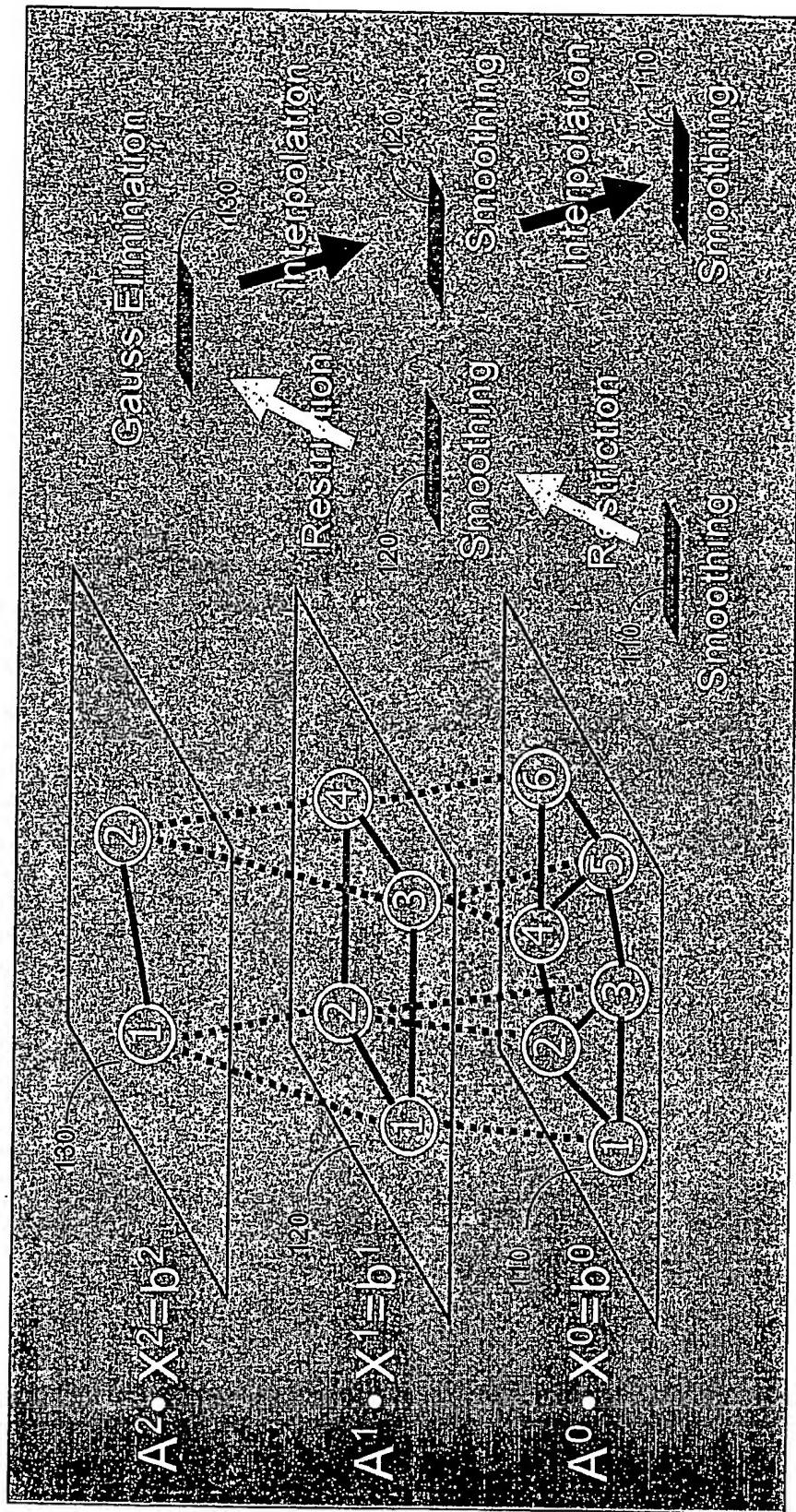
apply an algebraic multigrid method to a matrix  
representative of a circuit network to construct a plurality  
of matrices with different degrees of coarsening grids;

15 divide the circuit network into active regions and  
inactive regions according to circuit activities; and

perform an iterative smoothing operation in an active  
region more frequently than in an inactive region.

20 26. The article as in claim 25, wherein the machine-  
executable instructions further comprise instructions that  
cause the machine to perform an iterative smoothing operation  
to solve for a matrix equation of each grid and to map a  
computation result of each grid to a next finer or coarser  
25 grid until a residual error of a solution is less than a pre-  
determined threshold.

FIG. 1



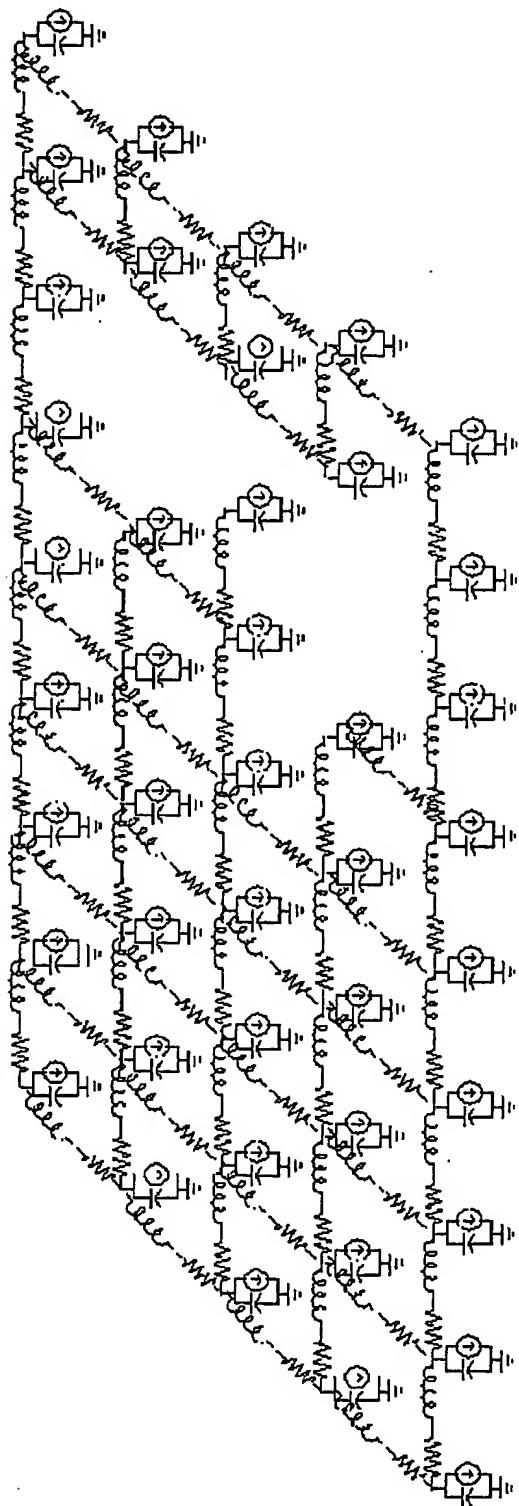
**FIG. 2**

FIG. 3B

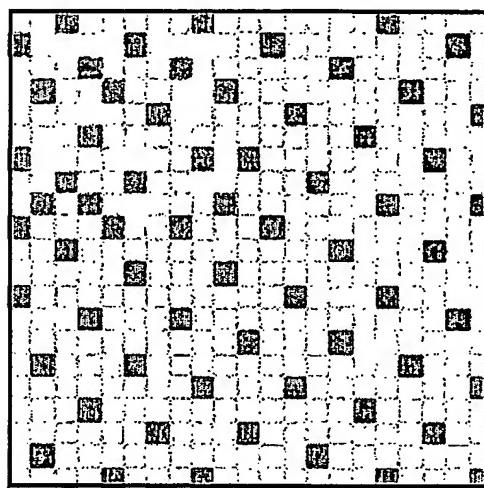


FIG. 3A

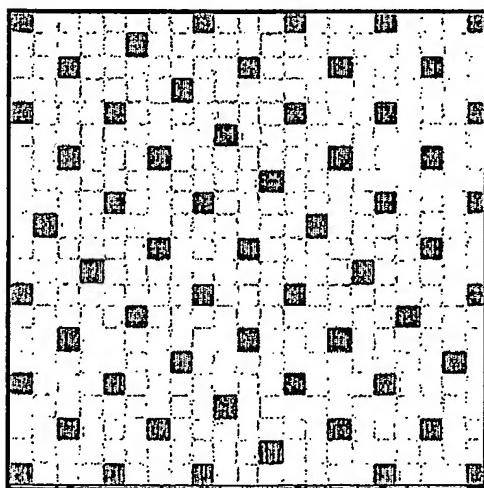
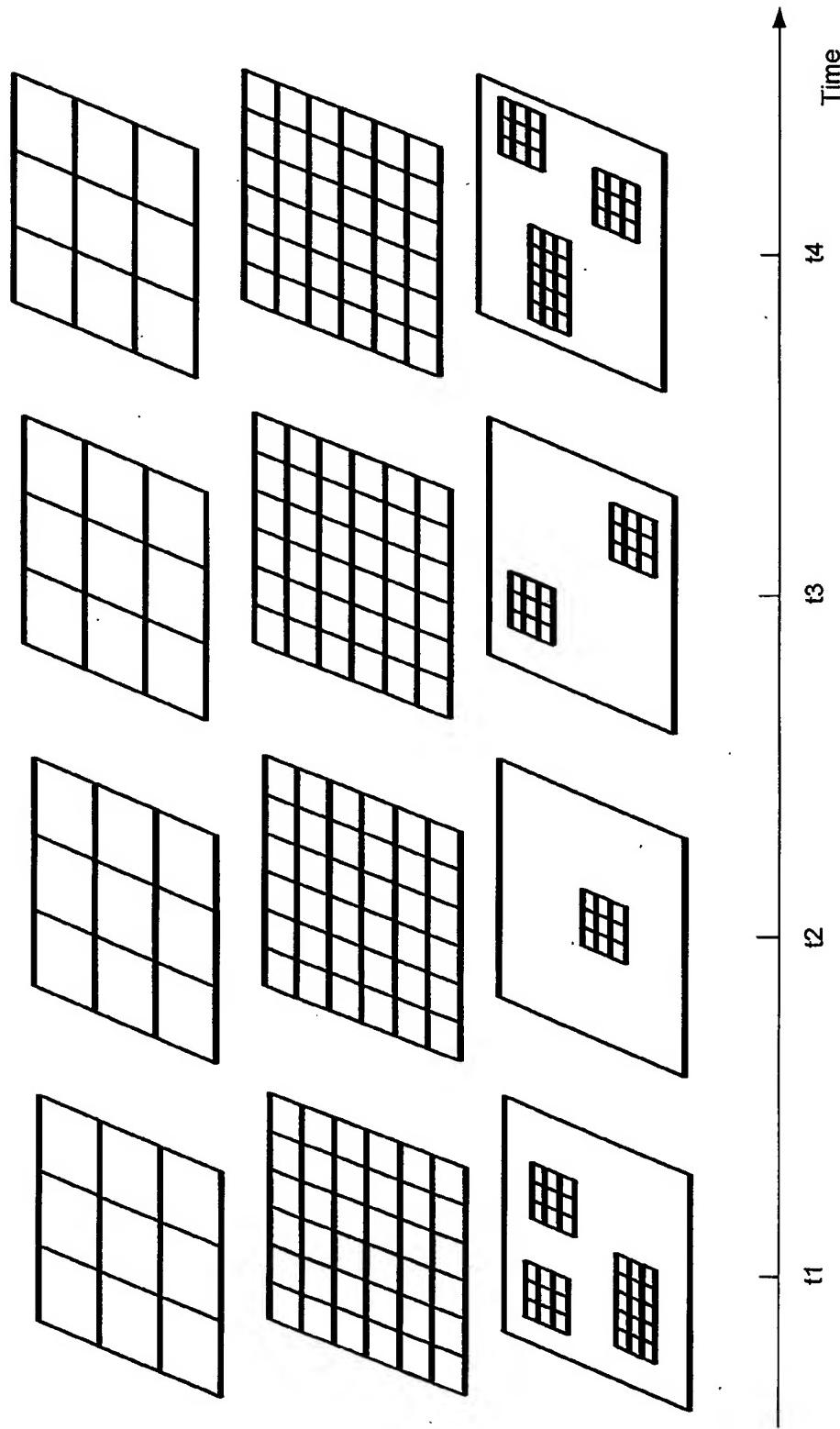
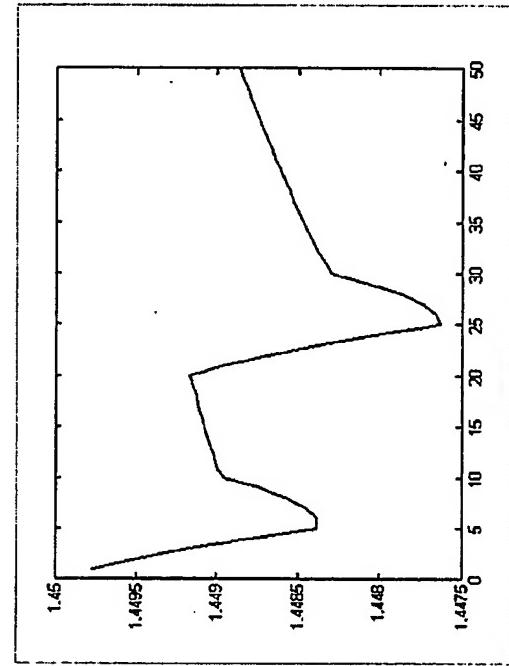
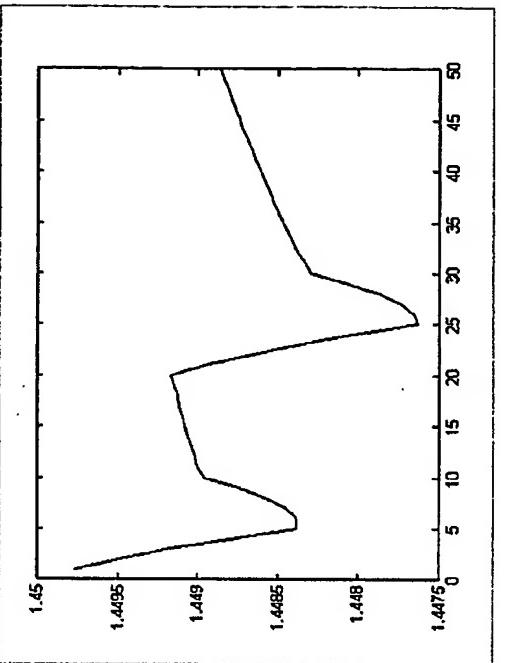


FIG. 4



CIRCUIT NETWORK ANALYSIS USING ALGEBRAIC  
MULTIGRID APPROACH**FIG. 5A****FIG. 5B**

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